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Sheet 1 of 1

Complete if Known	
Application Number	10/784,417
Filing Date	~~Herewith~~ 02/23/2004
First Named Inventor	Minchang Liang
Art Unit	2822
Examiner Name	SOWARD
Attorney Docket Number	A1385

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		A. HOKAZONO et al. "Source/Drain Engineering for Sub-100 nm CMOS Using Selective Epitaxial Growth Technique" (c) 2000 IEEE	
		A. SAMOILOV et al. "Properties and Applications of Strained Si/SiGe", Applied Materials Inc., April 17, 2002	
		J. ZHANG. et al."n-Si/i-p-i SiGe/n-Si structure for SiGe microwave power heterojunction bipolar transistor grown by ultra-high-vacuum chemical molecular epitaxy" Journal of Applied Physics, Vol 86, No. 3, pp. 1463-1466, 1 August 1999 (c) American Institute of Physics	
		M. KUMAR, "A 3-D BiCMOS Technology Using Selective Epitaxial Growth (SEG) and Lateral Solid Phase Epitaxy (LSPE)", (c) 2001 IEEE	
		J.-M. HARTMANN, "Reduced Pressure - Chemical Vapor Deposition of Si/SiGeC heterostructures for future applications", CEA/LETI Annual Review 2002	
		R. CHAU, "Advanced Depleted-Substrate Transistors: Single-Gate, Double-Gate and Tri-Gate", 2002 International Conference on Solid State Devices and Materials (SSDM 2002), Nagoya, Japan 9/17/02	
		Z. KRIVOKAPIC, "High Performance 25 nm FDSOI Devices with Extremely Thin Silicon Channel" AMD, Technology Research Group (6/2003)	

Examiner Signature	John M Soward	Date Considered	5-13-05

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